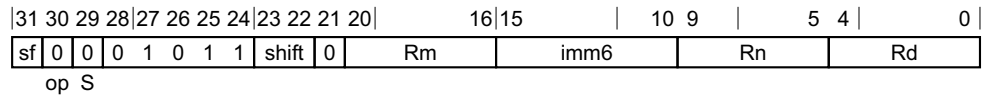


C5.6.5 ADD (shifted register)

Add (shifted register): $Rd = Rn + \text{shift}(Rm, \text{amount})$



32-bit variant (sf = 0)

ADD <Wd>, <Wn>, <Wm>{, <shift> #<amount>}

64-bit variant (sf = 1)

ADD <Xd>, <Xn>, <Xm>{, <shift> #<amount>}

```
integer d = UInt(Rd);
integer n = UInt(Rn);
integer m = UInt(Rm);
integer datasize = if sf == '1' then 64 else 32;
boolean sub_op = (op == '1');
boolean setflags = (S == '1');
```

```
if shift == '11' then ReservedValue();
if sf == '0' && imm6<5> == '1' then ReservedValue();
```

```
ShiftType shift_type = DecodeShift(shift);
integer shift_amount = UInt(imm6);
```

Assembler Symbols

<Wd>	Is the 32-bit name of the general-purpose destination register, encoded in the "Rd" field.								
<Wn>	Is the 32-bit name of the first general-purpose source register, encoded in the "Rn" field.								
<Wm>	Is the 32-bit name of the second general-purpose source register, encoded in the "Rm" field.								
<Xd>	Is the 64-bit name of the general-purpose destination register, encoded in the "Rd" field.								
<Xn>	Is the 64-bit name of the first general-purpose source register, encoded in the "Rn" field.								
<Xm>	Is the 64-bit name of the second general-purpose source register, encoded in the "Rm" field.								
<shift>	Is the optional shift type to be applied to the second source operand, defaulting to LSL and <table style="margin-left: 20px; border-collapse: collapse;"> <tr><td>LSL</td><td>when shift = 00</td></tr> <tr><td>LSR</td><td>when shift = 01</td></tr> <tr><td>ASR</td><td>when shift = 10</td></tr> <tr><td>RESERVED</td><td>when shift = 11</td></tr> </table>	LSL	when shift = 00	LSR	when shift = 01	ASR	when shift = 10	RESERVED	when shift = 11
LSL	when shift = 00								
LSR	when shift = 01								
ASR	when shift = 10								
RESERVED	when shift = 11								
<amount>	For the 32-bit variant: is the shift amount, in the range 0 to 31, defaulting to 0 and encoded in the "imm6" field.								
<amount>	For the 64-bit variant: is the shift amount, in the range 0 to 63, defaulting to 0 and encoded in the "imm6" field.								

Operation

```
bits(datasize) result;  
bits(datasize) operand1 = X[n];  
bits(datasize) operand2 = ShiftReg(m, shift_type, shift_amount);  
bits(4) nzcvc;  
bit carry_in;  
  
if sub_op then  
    operand2 = NOT(operand2);  
    carry_in = '1';  
else  
    carry_in = '0';  
  
(result, nzcvc) = AddWithCarry(operand1, operand2, carry_in);  
  
if setflags then  
    PSTATE.<N,Z,C,V> = nzcvc;  
  
X[d] = result;
```